FEB 06 2006
PATENT & TRADEMARK OFFICE

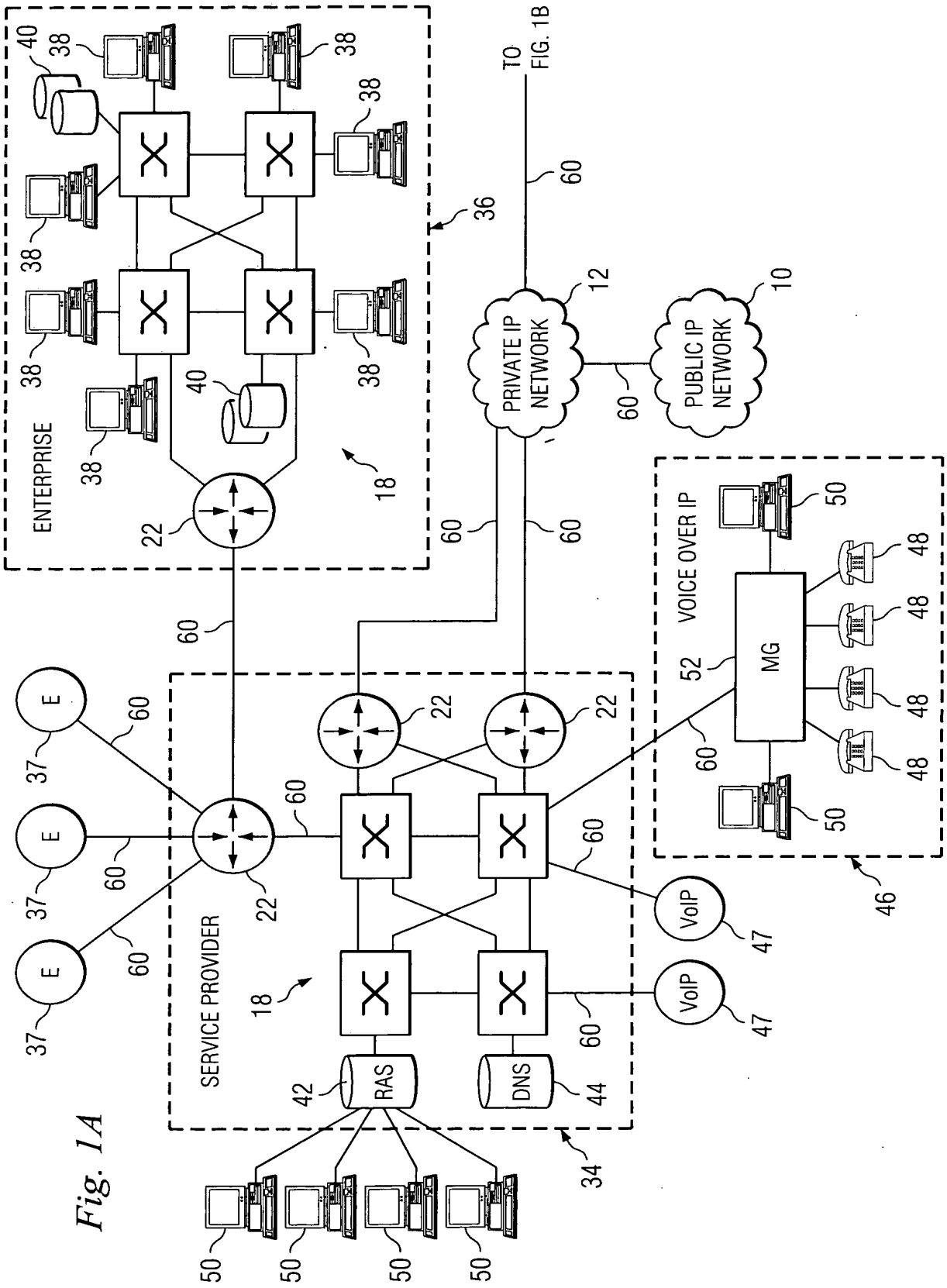


Fig. 1A

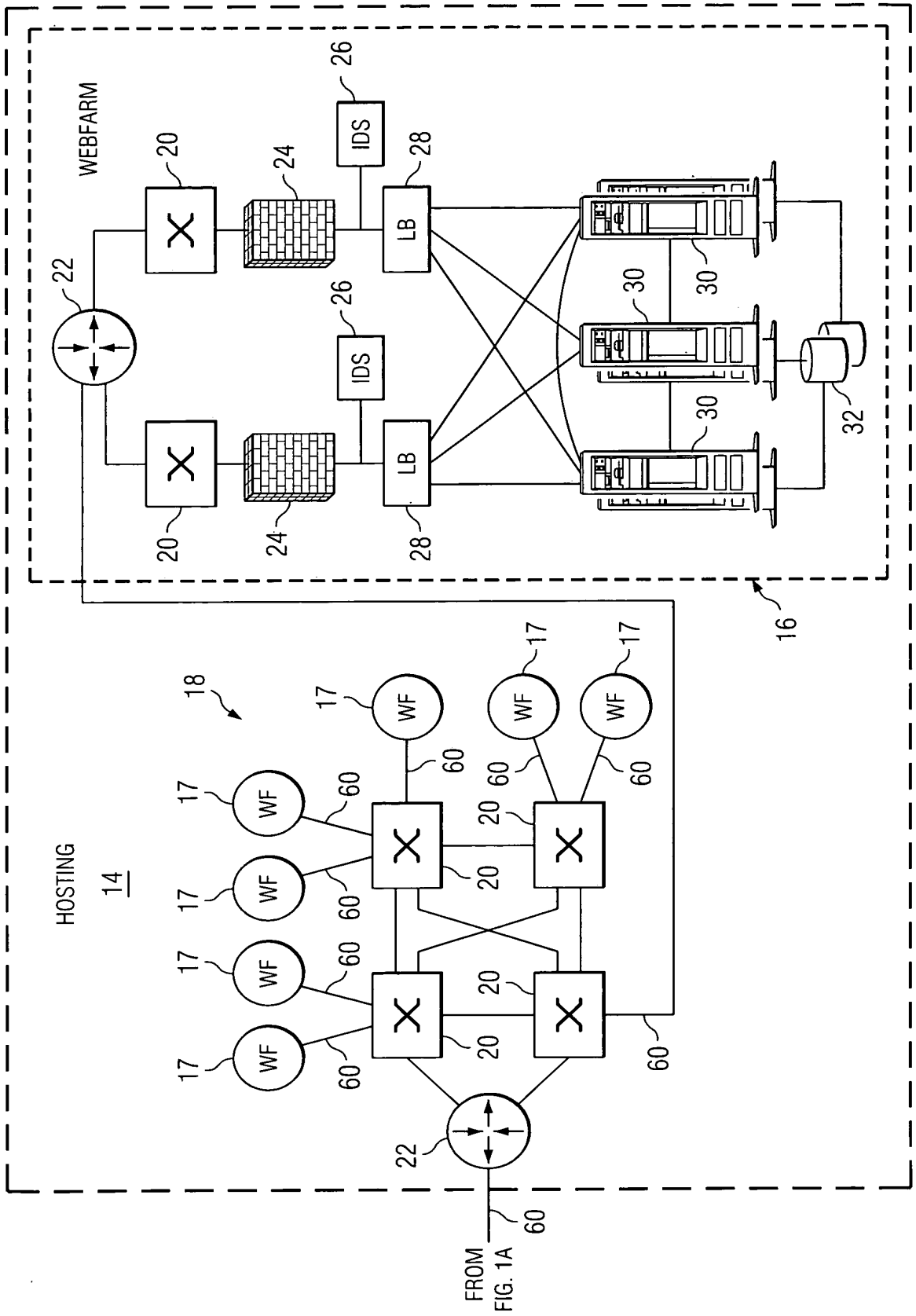


Fig. 1B

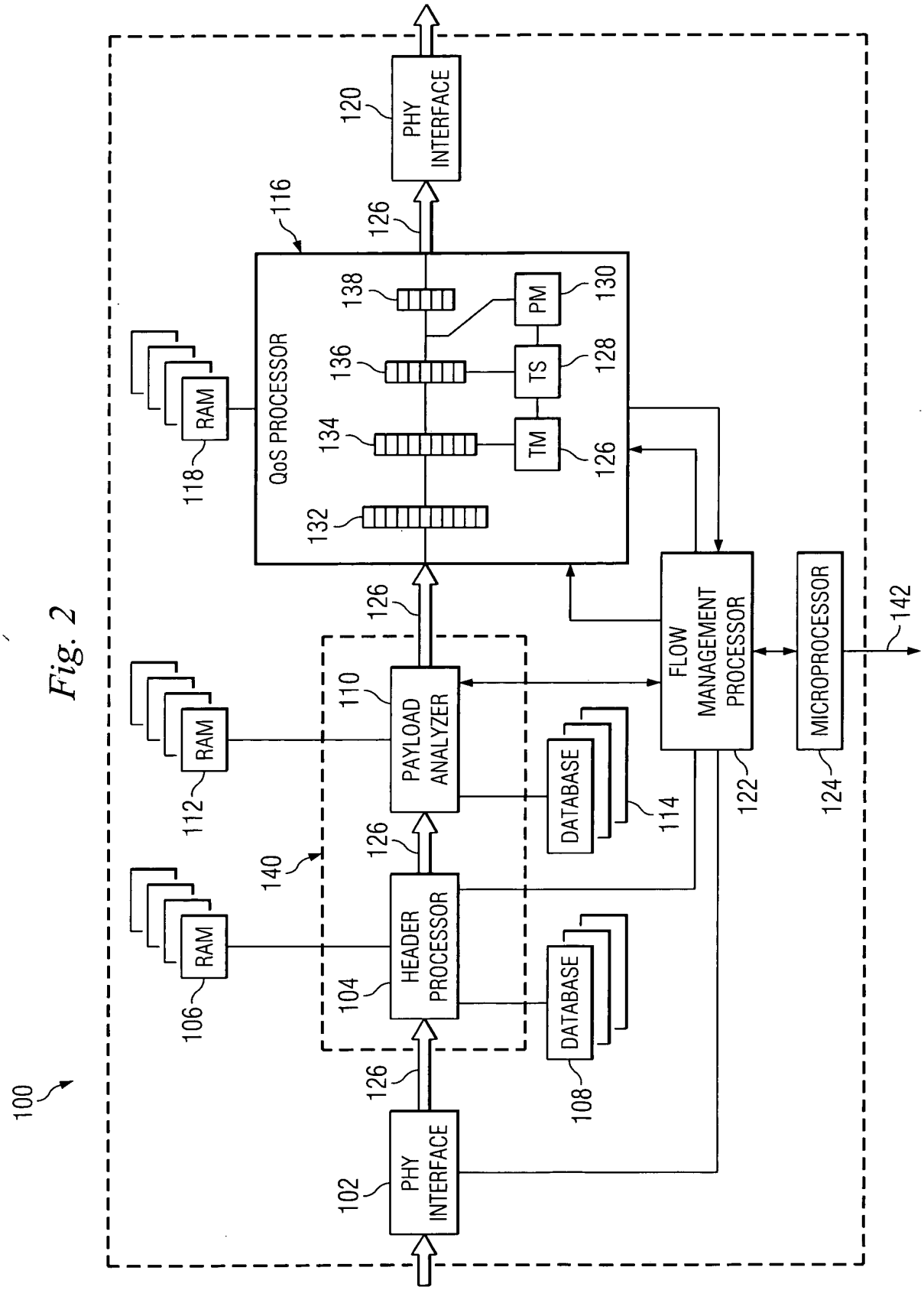

100
PHY INTERFACE
102
HEADER PROCESSOR
104
PAYLOAD ANALYZER
110
QoS PROCESSOR
116
FLOW MANAGEMENT PROCESSOR
122
MICROPROCESSOR
124
142
PHY INTERFACE
120
RAM
106
RAM
112
RAM
118
DATABASE
108
DATABASE
114
PM
130
TS
128
TM
126
126
126
126
126
126
126
132
134
136
138
140

Fig. 2

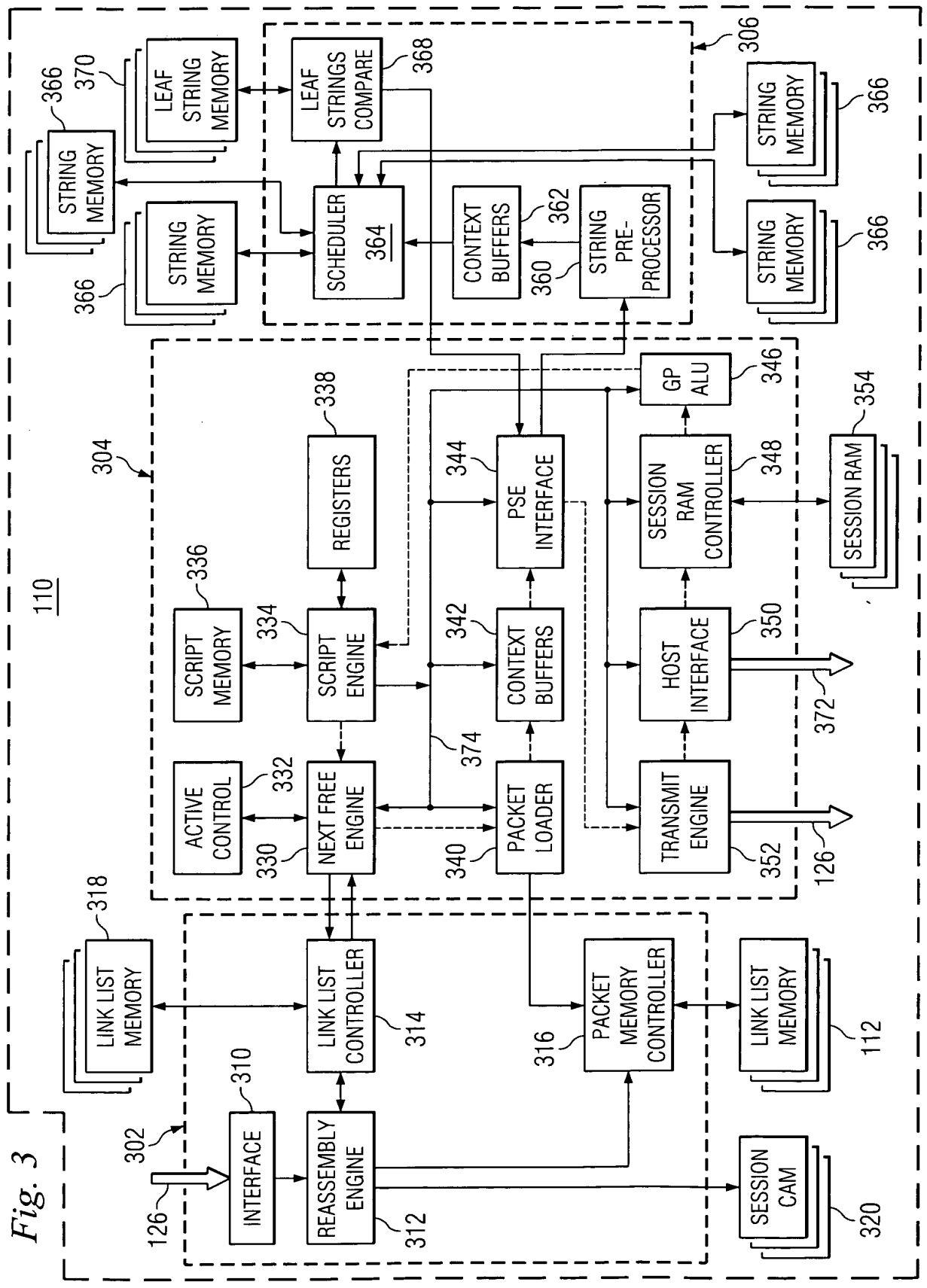

110
302
304
306
126
INTERFACE
REASSEMBLY ENGINE
312
310
LINK LIST CONTROLLER
314
LINK LIST MEMORY
318
PACKET MEMORY CONTROLLER
316
LINK LIST MEMORY
112
SESSION CAM
320
NEXT FREE ENGINE
330
ACTIVE CONTROL
332
SCRIPT ENGINE
334
SCRIPT MEMORY
336
REGISTERS
338
PACKET LOADER
340
CONTEXT BUFFERS
342
PSE INTERFACE
344
GP ALU
346
SESSION RAM CONTROLLER
348
SESSION RAM
354
HOST INTERFACE
350
372
TRANSMIT ENGINE
352
126
374
SCHEDULER 364
CONTEXT BUFFERS
360
362
STRING PRE-PROCESSOR
LEAF STRINGS COMPARE
368
LEAF STRING MEMORY
370
STRING MEMORY
366
STRING MEMORY
366
STRING MEMORY
366
STRING MEMORY
366

Fig. 3

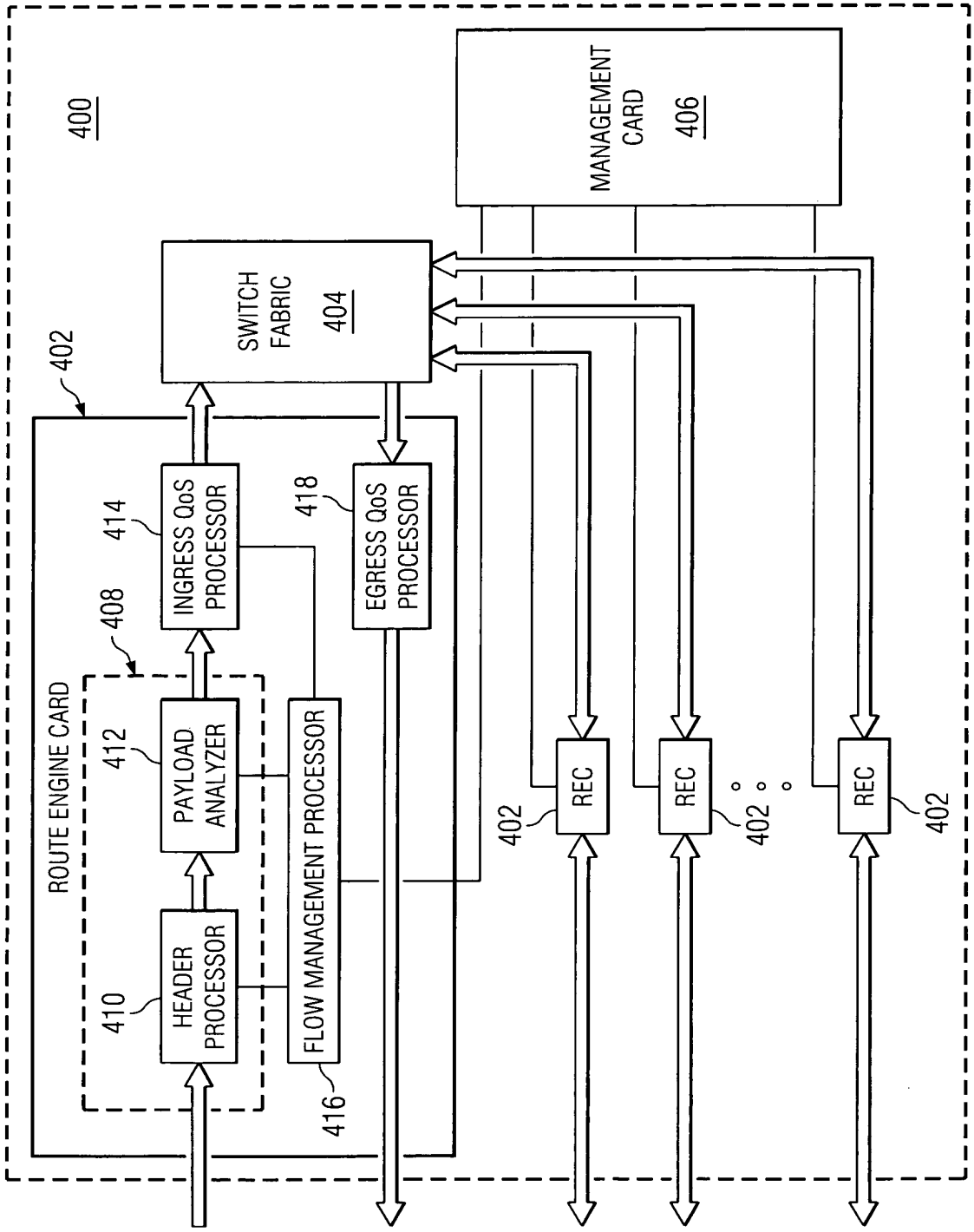
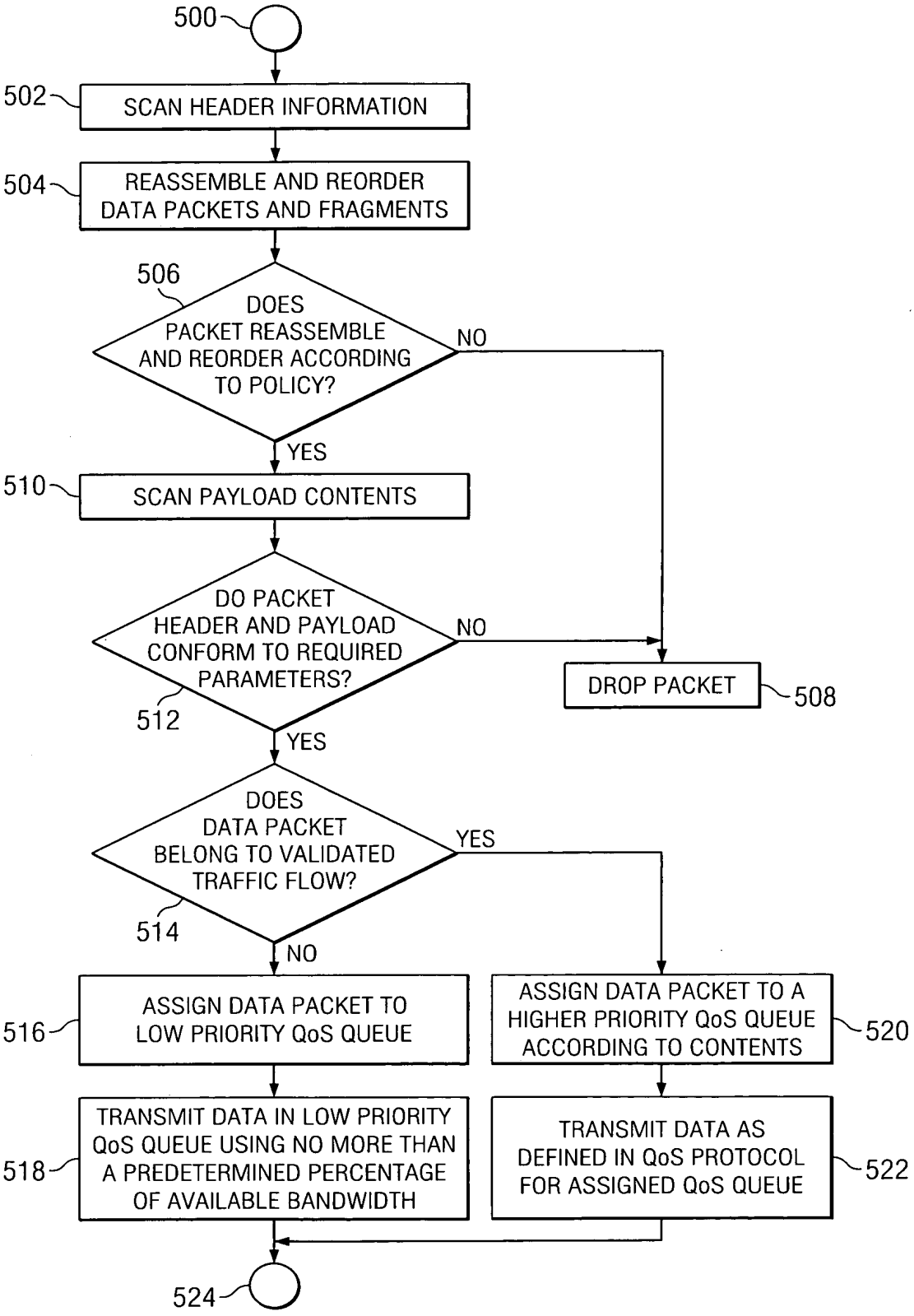

400
MANAGEMENT CARD 406
SWITCH FABRIC 404
402
INGRESS QoS PROCESSOR
414
418
EGRESS QoS PROCESSOR
408
ROUTE ENGINE CARD
412
PAYLOAD ANALYZER
FLOW MANAGEMENT PROCESSOR
410
HEADER PROCESSOR
416
REC
REC
REC
402
402
402

Fig. 4

Fig. 5


500
502
SCAN HEADER INFORMATION
504
REASSEMBLE AND REORDER DATA PACKETS AND FRAGMENTS
506
DOES PACKET REASSEMBLE AND REORDER ACCORDING TO POLICY?
NO
YES
510
SCAN PAYLOAD CONTENTS
DO PACKET HEADER AND PAYLOAD CONFORM TO REQUIRED PARAMETERS?
NO
512
DROP PACKET
508
YES
DOES DATA PACKET BELONG TO VALIDATED TRAFFIC FLOW?
YES
514
NO
516
ASSIGN DATA PACKET TO LOW PRIORITY QoS QUEUE
ASSIGN DATA PACKET TO A HIGHER PRIORITY QoS QUEUE ACCORDING TO CONTENTS
520
518
TRANSMIT DATA IN LOW PRIORITY QoS QUEUE USING NO MORE THAN A PREDETERMINED PERCENTAGE OF AVAILABLE BANDWIDTH
TRANSMIT DATA AS DEFINED IN QoS PROTOCOL FOR ASSIGNED QoS QUEUE
522
524